IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Efren M. Lacap et al.	Confirmation No.: 4089
Serial No.: 10/648,586	Art Unit: 1725
Filed: 26 August 2003	Examiner: Stoner, Kiley Shawn
Title: WAFER-LEVEL CHIP SCALE PACKAGE	Attorney Docket No.: 408204

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Dear Sir:

In accord with 37 C.F.R. 41.37, and fully responsive to the Office Action of 16 February 2007, Appellants hereby file this Appeal Brief in support of an appeal in the above-identified matter. A Notice of Appeal, with the appropriate fee of $250 as required by 37 C.F.R. 41.31(a)(1) and 41.20(b)(1) was filed on 16 May 2007. In accordance with 37 C.F.R. 41.37(a)(1) and 37 C.F.R. 1.136(a), this Appeal Brief is timely filed within three months of the filing of the Notice of Appeal.

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REAL PARTY IN INTEREST

The real party in interest for this appeal is Volterra Semiconductor Corporation, a corporation established under the laws of the State of Delaware and having a principle place of business at 3839 Spinnaker Court, Freemont, California 94538. Volterra Semiconductor Corporation is the assignee of United States Patent Application No. 10/648,586; evidence of such assignment was recorded on 26 August 2003, and may be found at reel/frame 014447/0295.

RELATED APPEALS AND INTERFERENCES

No other appeals or interferences are currently known to Appellants that will directly affect, be directly affected by, or have a bearing on the decision to be rendered by the Board of Patent Appeals and Interferences in the present appeal.

STATUS OF CLAIMS

Claims 1-17, 25-26, and 28-29 are pending in this application. Claims 1 is independent; claims 2-17, 25-26, and 28-29 all depend directly or indirectly from claim 1. Claims 12-17 were withdrawn from consideration.

Appellants appeal the rejection of claims 1-11, 25-26, and 28-29 under 35 U.S.C. 103(a). For purposes of this appeal, claims 1, 4, 5, 7, 8, 25, 26, and 28 stand on their own. Claims 2-3, 6, 9, 10, 11, and 29 stand or fall on their base claim.

STATUS OF AMENDMENTS

On 24 October 2005, a response to the 23 June 2005 office action was filed and entered. On 4 April 2006, a response to 4 January 2006 office action was filed and entered. On 22 November 2006, a response to the 23 May 2006 office action was filed and entered. An amendment (under 37 C.F.R. 41.33) responsive to the 16 February 2007 final office action was filed on 4 June 2007, and was entered for the purposes of appeal.

SUMMARY OF CLAIMED SUBJECT MATTER

Claim 1 is for a method of constructing a preformed solder bar made-ready-for installing a microchip to a corresponding circuit connection. A solder bar is illustrated in FIGS. 4 and 5 (reference characters 41 and 42), and FIGS. 7A, 7B, 8, and 10E (reference character 70). A

microchip, or a wafer, which may be part of a microchip, is illustrated in FIGS. 4 and 5 (reference character 50), FIGS. 7A and 7B (reference character 71), and FIGS. 8, 10A-10E (reference character 80); a corresponding circuit connection (e.g., a PCB trace) is illustrated in FIGS. 4 and 10E (reference characters 46A and 46B), and FIG. 6 (reference characters 62A-62D).

The method comprises forming a socket on a first surface of a microchip containing a wafer, as disclosed in paragraphs [0039], [0044], [0045], and [0047] of the specification and in FIG. 9 (reference characters 92-96), and FIGS. 10A-10B. A socket is illustrated in FIG. 4 (reference characters 37A and 37B), FIG. 5 (reference characters 47A and 47B), FIG. 8 (without a reference character specifically identifying the socket), and FIG. 10B (reference character 113). A microchip or wafer is illustrated in FIGS. 4 and 5 (reference character 50), FIGS. 7A and 7B (reference character 71), and FIGS. 8 and 10A-10E (reference character 80). The socket has predetermined physical dimensions complementary to those of a microchip connection pad footprint occupied by at least one contact pad area on the microchip, as disclosed in specification paragraph [0018]. The socket presents a conductive base capable of bonding to solder, as disclosed in specification paragraphs [0018] and [0045]. A conductive base consisting of UBM layers is illustrated in FIG. 4 (reference characters 42A and 42B) as well as in FIGS. 8 and 10A-10E (reference character 82). UBM is disclosed as being capable of bonding to solder in specification paragraph [0005].

The method further comprises forming a solder bar in substantially continuous contact with the conductive base to place the microchip in made-ready condition for installation prior to reflowing the solder for bonding to the circuit connection, as disclosed in specification paragraphs [0016], [0018], [0044]-[0047] as well as illustrated in FIG. 9 (reference characters 97-98) and FIGS. 10C-10D. The solder bar presents an elongate axis parallel to a plane of the footprint, and the solder bar fills the footprint, as illustrated in FIGS. 4-5, 8, and 10C-10E. The step of forming a socket includes depositing an adhesion layer onto the wafer via a screen printing process, as disclosed in specification paragraphs [0039] and [0045].

GROUNDS OF REJECTION TO BE REVIEWED UPON APPEAL

A) The rejection of claims 1-11 and 29 under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art ("AAPA") in view of U.S. Patent No. 6,372,622 to Tan et al. ("Tan") and U.S. Patent No. 4,808,274 to Nguyen ("Nguyen").

B) The rejection of claims 25-26 under 35 U.S.C. 103(a) as being unpatentable over AAPA, Tan, and Nguyen as applied to claim 1 and further in view of U.S. Patent No. 6,977,396 to Shen et al. ("Shen").

C) The rejection of claim 28 under 35 U.S.C. 103(a) as being unpatentable over AAPA, Tan, and Nguyen as applied to claim 1 and further in view of U.S. Patent Application Publication No. US 2003/0157789 to Tong et al. ("Tong").

ARGUMENTS

I. THE REJECTION OF CLAIMS 1-11 AND 29 UNDER 35 U.S.C. 103(a) OVER AAPA, TAN, AND NGUYEN SHOULD BE REVERSED BECAUSE THE EXAMINER HAS NOT ESTABLISHED A PRIMA FACIE CASE OF OBVIOUSNESS.

"During patent examination the PTO bears the initial burden of presenting a *prima facie* case of unpatentability." *In re Glaug*, 283 F.3d 1335, 1338 (Fed. Cir. 2002); *accord In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992). "If the PTO fails to meet this burden, then the applicant is entitled to the patent." *In re Glaug* at 1338; *accord In re Oetiker* at 1445. To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981 (CCPA 1974); codified in MPEP 2143.03. Furthermore, if the Examiner modifies or combines references to establish a *prima facie* case of obviousness, the Examiner must show "some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references." *In re Fine*, 837 F.2d 1071, 1074 (Fed. Cir. 1988); codified in MPEP 2143. The Examiner has not established a *prima facie* case of obviousness of Claims 1-11 and 29 because the Examiner has not met either of these requirements, as discussed below. For at least these reasons, the rejection of claims 1-11 and 29 should be reversed.

A. The Examiner Has Not Cited to Where All of the Elements of Claims 1-11 and 29 are Taught or Suggested in the Cited References.

Claim 1 recites a method of constructing a preformed solder bar made-ready-for installing a microchip to a corresponding circuit connection, comprising:

(a) forming a socket on a first surface of a microchip containing a wafer, such that the socket has predetermined physical dimensions complementary to those of a microchip connection pad footprint occupied by at least one contact pad area on the microchip, the socket presenting a conductive base capable of bonding to solder; and

(b) forming a solder bar in substantially continuous contact with the conductive base to place the microchip in made-ready condition for installation prior to reflowing the solder for bonding to the circuit connection,

(c) the solder bar presenting an elongate axis parallel to a plane of the footprint, the solder bar filling the footprint, and

(d) the step of forming a socket including depositing an adhesion layer onto the wafer via a screen printing process.

Step (b) of claim 1 requires, among other things, forming a *solder bar* in substantially continuous contact with the conductive base. The Examiner appears to argue that AAPA discloses forming a solder bar by stating that AAPA discloses "forming a solder layer (figure 2, items 3a, 3b, 3c where the layer comprises discrete units of solder balls) in substantially continuous contact with the conductive base" and "the examiner interprets the solder ball to be a thin solder bar." Office Action of 16 February 2007, page 2 (emphasis added). Appellants respectfully disagree that AAPA discloses forming a solder bar, as required by step (b) of claim 1.

First, nowhere in FIG. 2 or its description is disclosed forming any sort of solder structure. Second we respectfully assert that solder balls 3A, 3B, and 3C of FIG. 2 are not solder bars, and AAPA does not disclose solder bars. The Examiner argues that a solder bar is disclosed by solder balls 3A, 3B, and 3C by stating that (1) "pending claims must be 'given the broadest reasonable interpretation,'" and (2) that "DICTIONARY.COM defines 'bar' as a 'a structural or mechanical member,'" which reads on solder balls 3A, 3B, and 3C. *See* Office Action of 16 February 2007, page 5.

With respect to the Examiner's first argument, we note that pending claims must be given their broadest reasonable interpretation consistent with the specification. MPEP 2111 (emphasis added); *accord Phillips v. AWH Corp.*, 415 F.3d 1303, 1316 (Fed. Cir. 2005). Appellants respectfully assert that solder bars are distinguished from solder balls in the specification. For example, see paragraphs [0013], [0019], [0038], [0041], [0042], and [0051]-[0053] of the

specification. Therefore, to interpret the solder bar of claim 1 to read on solder balls 3A, 3B, and 3C is inconsistent with the specification, and therefore, an improper interpretation of claim 1.

With respect to the Examiner's second argument, we note that as of 10 July 2007, the entry in DICTIONARY.COM that the Examiner appears to refer to defines the word bar as a "relatively long, straight, rigid piece of solid material *used* as a fastener, support, barrier, or structural or mechanical member" (emphasis added). Therefore, the DICTIONARY.COM entry states that a bar may be used as a structural or mechanical member – a bar is not defined as a structural or mechanical member as argued by the Examiner.

The Examiner additionally implicitly argues that Tan discloses a solder rectangle, which the Examiner apparently equates to Appellants' solder bar. *See* Office Action of 16 February 2007, pages 3-4. Appellants respectfully assert that Tan does not disclose forming a solder bar as required by step (b) of claim 1. Tan discloses forming a solder bump with increased solder volume using two separate openings in one or more masking or resist layers. The first opening, which is closest to the bond pad of a semiconductor device, is used for stud plating. The second opening, which at least partially overlies the first opening, is used for forming a solder bump. The use of two openings in the masking or resist layers may allow the formation of solder bumps having a larger volume than that of some prior art solder bumps. *See* e.g., Tan col. 2, lines 15-67; col. 3, lines 1-19. The solder bumps are reflowed to form "substantially spherical reflowed solder bumps", Tan, col. 5, lines 6-15 (emphasis added). Thus, Tan essentially discloses forming solder balls that purportedly may have a larger volume than other solder balls.

Accordingly, the Examiner has not shown forming a solder bar, as required by step (b) of claim 1, to be taught or suggested in the cited references.

Step (b) of claim 1 further requires that the step of forming a solder bar place the microchip in made-ready condition for installation prior to reflowing the solder for bonding to the circuit connection. The Examiner argues that item 3A of Appellants' FIG. 2 discloses placing the microchip in made-ready condition for installation. Office Action of 16 February 2007, page 2. Appellants respectfully direct the Board's attention to the fact that item 3A of FIG. 2 is a reflowed solder ball. In the case of FIG. 2, the microchip 4 is already installed on PCB 1, as

acknowledge by the Examiner on page 5 of the Office Action of 16 February 2007. Accordingly, reflowed solder ball 3A cannot disclose a microchip in made-ready condition for installation prior to reflowing the solder. Although the Examiner acknowledges that FIG. 2 illustrates a microchip that is already installed on a PCB (Office Action of 16 February 2007, page 5), the Examiner argues "[i]t is the [E]xaminer's position that the preformed solder bar chip package 'makes it ready' for installation in its ultimate use in the electronic product," Office Action of 16 February 2007, page 6. First, Appellants note that this argument contradicts the Examiner's earlier acknowledgment that the microchip is already installed. Second, Appellants respectfully assert that the Examiner's argument that the preformed solder bar chip package 'makes it ready' for installation in its ultimate use does not address the requirement of step (b) of claim 1 that the step of forming a solder bar place the microchip in made-ready condition for installation prior to reflowing the solder for bonding to the circuit connection.

Accordingly, the Examiner has not shown that the step of forming a solder bar place the microchip in made-ready condition for installation prior to reflowing the solder for bonding to the circuit connection, as required by step (b) of claim 1, to be taught or suggested in the cited references.

Step (c) of claim 1 recites the solder bar presenting an elongate axis parallel to a plane of the footprint, the solder bar filling the footprint. However, the Examiner's arguments with respect to claims 1-11 and 29 do not address this step. Accordingly, the Examiner has not shown that the cited references teach or disclose the solder bar presenting an elongate axis parallel to a plane of the footprint, the solder bar filling the footprint, as required by claim 1.

For at least these reasons, the Examiner has not shown the cited references to teach or suggest each element of claim 1. Therefore, the Examiner has not shown a *prima facie* case of obviousness of claim 1, and the rejection of claim 1 should be reversed.

The rejection of claims 2-11 and 29 is deficient for at least the reasons cited above because claims 2-11 and 29 depend directly or indirectly from claim 1. If an independent claim is nonobvious under 35 U.S.C. 103 then any claim depending therefrom is nonobvious. *In re*

Fine, 837 F.2d 1071, 1076 (Fed. Cir. 1988); codified in MPEP 2143.03. Therefore, the rejection of claims 2-11 and 29 should be reversed at least for this reason.

With respect to claim 4 specifically, the rejection further fails to establish that the cited references teach or suggest that the step of depositing the UBM material includes depositing a conductor selected from at least one of titanium, tungsten, tin, aluminum, gold, silver, and lead. The Examiner argues that this is disclosed in paragraph [0008] of the specification as AAPA. Office Action of 16 February 2007, page 3. However, paragraph [0008] in no manner teaches or suggests anything regarding UBM material. Accordingly, the Examiner has not established a *prima facie* case of obviousness of claim 4, and the rejection of claim 4 should be reversed.

With respect to claim 5 specifically, the rejection further fails to establish that the cited references to teach or suggest that the step of forming the socket includes forming the socket such that the socket has predetermined dimensions complementary to a microchip connection pad footprint having a geometry selected from the group consisting of "E," "L," and "U" shapes. The Examiner appears to address claim 5 by arguing that the side profile of item 29 of figure 2 discloses "wherein the step of forming the socket includes the predetermined dimensions selected from the group consisting of rectangular, 'E', 'L,' and 'U' shapes." Office Action of 16 February 2007, page 3. The Examiner further argues that a "U shape is clearly visible from figure 2" and includes a copy of FIG. 2 from Appellants' application, a copy of which is reproduced below. Office Action of 16 February 2007, page 6.

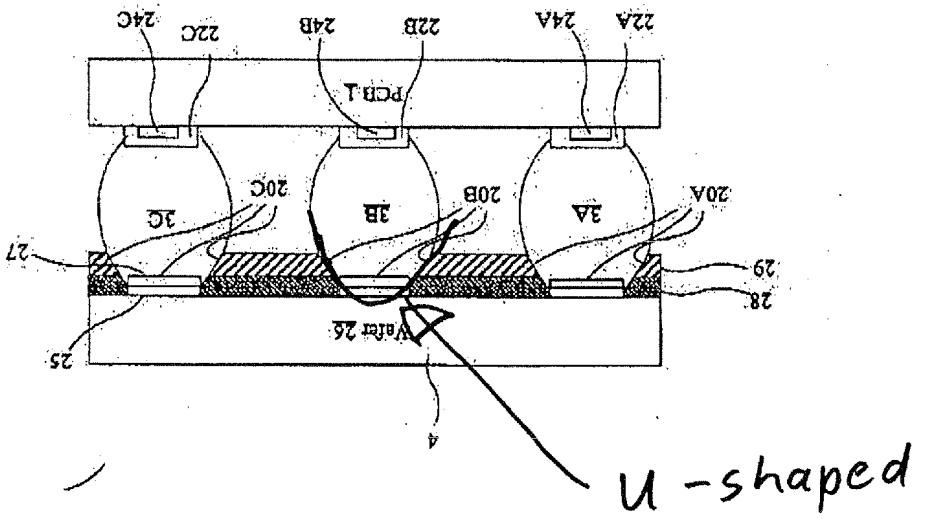

Figure from page 6 of Office Action of 16 February 2007

As can be seen in the figure above, the Examiner has hand-drawn a U-shape on Appellants' FIG. 2. Appellants respectfully assert that the Examiner's addition of a U-shape to FIG. 2 does not show that FIG. 2 discloses any sort of U-shape. To the contrary, the Examiner's U-shape is at odds with the geometry of FIG. 2; for example, UBM 27 and adhesion layer 25 conflict with the Examiner's U-shape. Therefore, the Examiner's hand-drawn U-shape does not reflect the actual geometry of the sockets of FIG. 2. Accordingly, the Examiner has not shown a *prima facie* case of obviousness of claim 5, and the rejection of claim 5 should be reversed.

With respect to claim 7 specifically, the rejection further fails to establish that the cited references teach or suggest that the step of forming the solder bar comprises forming a solder bar having a planar rectilinear configuration wherein a plane of the solder bar is parallel to the socket and the elongate axis. Appellants respectfully assert that the Examiner's arguments with respect to claims 1-11 and 29 do not address forming a solder bar having a planar rectilinear configuration wherein a plane of the solder bar is parallel to the socket and the elongate axis. Accordingly, the Examiner has not shown a *prima facie* case of obviousness of claim 7, and the rejection of claim 7 should be reversed.

With respect to claim 8 specifically, the rejection further fails to establish that the cited references teach or suggest that the step of forming the solder bar comprises forming a solder bar having a planar curvilinear configuration wherein a plane of the solder bar is parallel to the socket and the elongate axis. Appellants respectfully assert that the Examiner's arguments with respect to claims 1-11 and 29 do not address forming a solder bar having a planar curvilinear configuration wherein a plane of the solder bar is parallel to the socket and the elongate axis. Accordingly, the Examiner has not shown a *prima facie* case of obviousness of claim 8, and the rejection of claim 8 should be reversed.

B. The Examiner Has Not Cited Any Teaching or Suggestion to Modify or Combine the Cited References in the Manner Suggested by the Examiner.

As stated above, to establish a *prima facie* case of obviousness by combining references and/or by modifying a reference, the Examiner must show some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead an individual to combine the references and/or modify the reference. This showing "must be based on objective evidence of record." *In re Lee*, 277 F.3d 1338, 1343 (Fed. Cir. 2002). The Examiner argues that "Tan teaches the interchangeability between a solder ball and a solder rectangle" and further states it "would have been obvious to one of ordinary skill in the art at the time of the invention to modify the shape of the solder to utilize a rectangle in order to form a reliable electrical connection" and cites Tan as support. Office Action of 16 February 2007, pages 3-4.

Tan discloses that openings in a masking or resist layer can have various shapes (Tan, col. 4, lines 25-29); however, this is not the same as stating a solder ball and solder rectangle are interchangeable. Tan also discloses forming a solder bump having a larger volume than prior art solder bumps to increase a standoff distance between a semiconductor device and a substrate; Tan states that increasing the standoff distance may increase reliability. *See* e.g., Tan col. 2, lines 15-67; col. 3, lines 1-19. However, contrary to the Examiner's argument, Tan does not teach or suggest that a solder rectangle provides a more reliable electrical connection than a solder ball. Accordingly, the Examiner has not shown there to be a teaching or suggestion to

modify AAPA according to Tan. Therefore, the rejections of claim 1-11 and 29 should be reversed for at least this reason.

II. THE REJECTION OF CLAIMS 25-26 UNDER 35 U.S.C. 103(a) OVER AAPA, TAN, NGUYEN, AND SHEN SHOULD BE REVERSED BECAUSE THE EXAMINER HAS NOT ESTABLISHED A PRIMA FACIE CASE OF OBVIOUSNESS.

Claims 25 and 26 are nonobvious because they depend from claim 1 which is nonobvious as argued above. Furthermore, the rejection fails to establish that the cited references teach or suggest (1) forming a socket such that one of a depth and a width of the socket is at least twice the other of the depth and the width, and (2) forming a solder bar with a width or a depth that is at least four times the height of the solder bar, as recited by claims 25 and 26, respectively. *See* Office Action of 16 February 2007, page 4. Therefore, the Examiner has not shown a *prima facie* case of obviousness of claims 25 and 26. For at least these reasons, their rejection should be reversed.

III. THE REJECTION OF CLAIM 28 UNDER 35 U.S.C. 103(a) OVER AAPA, TAN, NGUYEN, AND TONG SHOULD BE REVERSED BECAUSE THE EXAMINER HAS NOT ESTABLISHED A PRIMA FACIE CASE OF OBVIOUSNESS.

The rejection of claim 28 is deficient for at least the reasons cited above because claim 28 depends from claim 1. Furthermore, the rejection fails to show an objective teaching in the cited references or that knowledge generally available to one of ordinary skill in the art would lead an individual to combine Tong with AAPA, Tan, and Nguyen. The Examiner states "[i]t would have been obvious to one of ordinary skill in the art at the time of the invention to modify the layers to utilize the claimed deposition process in order to ensure the layers are adequately formed" and refers to "Tong col. 10-32" as support. Appellants respectfully assert that this justification for combining references is a conclusory statement and not based objective evidence of record. The reference to Tong is unintelligible because Tong contains fewer than 32 columns, and Tong does not state that using a sputtering process ensures that layers are adequately formed. Accordingly, the Examiner has not established a *prima facie* case of obviousness of claim 28. For at least these reasons, the rejection of claim 28 should be reversed.

REFERENCE TO CLAIMS APPENDIX

Appellants provide a copy of the claims involved in this appeal, on separate pages as an appendix hereto in accordance with 37 CFR 41.37(c)(iii).

REFERENCE TO EVIDENCE APPENDIX

Although Appellants offer no additional evidence, a page titled "Evidence Appendix" is provided on a separate page as an appendix hereto in accordance with 37 CFR § 41.37 (c)(ix).

REFERENCE TO RELATED PROCEEDINGS APPENDIX

To Appellants' knowledge, there are no decisions rendered by a court or the Board for submission with this appeal. A page entitled "Related Proceedings Appendix" is provided on a separate page as an appendix hereto in accordance with 37 CFR § 41.37 (c)(x).

CONCLUSION

Appellants respectfully submit that the Examiner has not presented a *prima facie* case of unpatentability of claims 1-11, 25-26, and 28-29 under 35 U.S.C. 103(a). Other than a $60.00 fee for a one-month extension of time, we believe no additional fees are due in connection with this matter. However, if any additional fee is deemed necessary, the Commissioner is authorized to charge any such fee to deposit account 12-0600, referencing the Attorney Docket Number 408204.

Respectfully submitted,

By: Philip diZerega

Philip diZerega, Reg. No. 57,892
LATHROP & GAGE L.C.
4845 Pearl East Circle, Suite 300
Boulder, CO 80301
Telephone: (720) 931-3037
Facsimile: (720) 931-3001

CLAIM APPENDIX

1. (Previously Presented) A method of constructing a preformed solder bar made-ready-for installing a microchip to a corresponding circuit connection, comprising:

forming a socket on a first surface of a microchip containing a wafer, such that the socket has predetermined physical dimensions complementary to those of a microchip connection pad footprint occupied by at least one contact pad area on the microchip, the socket presenting a conductive base capable of bonding to solder; and

forming a solder bar in substantially continuous contact with the conductive base to place the microchip in made-ready condition for installation prior to reflowing the solder for bonding to the circuit connection,

the solder bar presenting an elongate axis parallel to a plane of the footprint, the solder bar filling the footprint, and

the step of forming a socket including depositing an adhesion layer onto the wafer via a screen printing process.

2. (Previously Presented) The method of claim 1, wherein the wafer is a silicon wafer and the step of forming the socket further comprises

depositing under-bump-metallization (UBM) material contacting the adhesion layer to complete formation of the conductive base.

3. (Original) The method of claim 2, wherein the step of depositing the adhesion layer includes depositing a conductor selected from the group consisting of aluminum, nickel-vanadium, titanium, tungsten and copper.

4. (Previously Presented) The method of claim 2, wherein the step of depositing the UBM material includes depositing a conductor selected from at least one of titanium, tungsten, tin, aluminum, gold, silver, and lead.

5. (Previously Presented) The method of claim 1, wherein the step of forming the socket includes forming the socket such that the socket has predetermined dimensions complementary to a microchip connection pad footprint having a geometry selected from the group consisting of "E," "L," and "U" shapes.

6. (Original) The method of claim 1, wherein the step of forming the socket includes the physical dimensions selected from the group consisting of ring, square, and circular shapes.

7. (Previously Presented) The method of claim 1, wherein the step of forming the solder bar comprises forming a solder bar having a planar rectilinear configuration wherein a plane of the solder bar is parallel to the socket and the elongate axis.

8. (Previously Presented) The method of claim 1, wherein the step of forming the solder bar comprises forming a solder bar having a planar curvilinear configuration wherein a plane of the solder bar is parallel to the socket and the elongate axis.

9. (Previously Presented) The method of claim 1, the step of forming the socket comprising a step of forming a passivation layer on substantially all of the first surface, exclusive of an area where the socket is located.

10. (Previously Presented) The method of claim 9, wherein the step of forming the passivation layer includes the steps of:

applying one or more layers of passivation material to the entire first surface; and

removing a selected portion of the passivation material from an area where the socket is to be located.

11. (Previously Presented) The method of claim 10, wherein the step of applying one or more layers of passivation material includes applying at least one layer selected from the group consisting of polysilicon, silicon dioxide, silicon nitride, oxynitride, polyimide and benzocyclobutane.

12. (Withdrawn – Previously Presented) The method of claim 1, further comprising depositing a non-solder base metal in the socket after the step of forming the socket and prior to the step of forming the solder bar, such that the solder bar contains the non-solder base metal and the solder in respective layers.

13. (Withdrawn) The method of claim 12, wherein the step of depositing the non-solder base metal includes electroplating the non-solder base metal.

14. (Withdrawn) The method of claim 12, wherein the step of depositing the non-solder base metal includes screen printing at least one base metal layer.

15. (Withdrawn) The method of claim 14, wherein the step of depositing the non-solder base metal includes depositing a layer selected from the group consisting of copper, gold, platinum, palladium, silver, aluminum, tin, bismuth, lead, titanium, tungsten, vanadium and alloys thereof.

16. (Withdrawn – Previously Presented) The method of claim 1, wherein the step of forming the solder bar includes electroplating one or more solder layers.

17. (Withdrawn – Previously Presented) The method of claim 1, wherein the step of forming the solder bar includes screen printing one or more solder layers.

18 - 24. (Canceled)

25. (Previously Presented) The method of claim 1, wherein forming a socket comprises forming the socket such that one of a depth and a width of the socket is at least twice the other of the depth and the width.

26. (Previously Presented) The method of claim 1, wherein forming the solder bar comprises forming the solder bar with a width or a depth that is at least four times the height of the solder bar.

27. (Canceled)

28. (Previously Presented) The method of claim 2, wherein depositing under-bump-metallization (UBM) material comprises sputtering the UBM material.

29. (Previously Presented) The method of claim 1, wherein the corresponding circuit connection comprises one of a PCB, another microchip, and a ceramic interposer.

EVIDENCE APPENDIX

NONE

RELATED PROCEEDINGS APPENDIX

NONE